

**Preliminary Amendment**

Applicant: Bernd Betz et al.

Serial No.: Unknown

(Priority Application No. DE 103 48 715.8 )

(International Application No. PCT/DE2004/002199)

Filed: Herewith

(Priority Date: October 16, 2003 )

(International Filing Date: October 1, 2004)

Docket No.: I431.155.101/FIN 527 PCT/US

Title: PROCESS FOR PRODUCING AND APPARATUS FOR IMPROVING THE BONDING BETWEEN A PLASTIC AND A METAL

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**IN THE CLAIMS**

Please cancel claims 1-15 without prejudice.

Please add claims 16-41 as follows:

**WHAT IS CLAIMED IS:**

1-15. (Cancelled)

16. (New) A process for producing a leadframe configured to be fitted with a semiconductor chip and to be encapsulated with a plastic compound, the process comprising:  
providing a leadframe;

applying an interlayer attackable by an etchant that comprises one or more individual layers, to the leadframe; and

etching into the surface of the interlayer using the etchant.

17. (New) The process as claimed in claim 16, comprising depositing silver, a silver alloy and/or a silver compound and/or nickel for the interlayer by means of chemical or electrodeposition processes.

18. (New) The process as claimed in claim 16, comprising applying silver, a silver alloy and/or a silver compound and/or nickel as a coarse deposit for the interlayer.

19. (New) The process as claimed in claim 16, comprising applying the interlayer in the form of one or more individual layers each having a uniform composition.

20. (New) The process as claimed in claim 16, comprising wherein the etching is effected as grain boundary etching at the surface of the interlayer and/or is carried out by selectively etching out at least one of the alloying constituents or the compound components of the silver at the surface of the interlayer.

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21. (New) The process as claimed in claim 16, comprising wherein the application of the interlayer and the etching are both carried out over the entire surface of the leadframe.

22. (New) The process as claimed in claim 16, comprising wherein both the application of the interlayer and the etching are carried out selectively at defined locations of the surface of the leadframe.

23. (New) A process for producing a semiconductor device, comprising:  
producing a leadframe including, providing the leadframe, applying an interlayer attackable by an etchant that comprises one or more individual layers, to the leadframe, and etching into the surface of the interlayer using the etchant;  
placing a semiconductor chip onto the leadframe; and  
applying a plastic compound as encapsulating housing to the leadframe and semiconductor chip.

24. (New) The process as claimed in claim 23, comprising depositing silver, a silver alloy and/or a silver compound and/or nickel for the interlayer by means of chemical or electrodeposition processes.

25. (New) The process as claimed in claim 23, comprising applying silver, a silver alloy and/or a silver compound and/or nickel as a coarse deposit for the interlayer.

26. (New) The process as claimed in claim 23, comprising applying the interlayer in the form of one or more individual layers each having a uniform composition.

27. (New) The process as claimed in claim 26, comprising wherein the etching is effected as grain boundary etching at the surface of the interlayer and/or is carried out by

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selectively etching out at least one of the alloying constituents or the compound components of the silver at the surface of the interlayer.

28. (New) The process as claimed in claim 27, comprising wherein the application of the interlayer and the etching are both carried out over the entire surface of the leadframe; and wherein both the application of the interlayer and the etching are carried out selectively at defined locations of the surface of the leadframe.

29. (New) A leadframe configured to fit with a semiconductor chip and to be encapsulated with a plastic compound, the leadframe comprising:  
a metallic single-piece base body of a leadframe,  
at least one interlayer which has been applied to the base body and may comprise one or more individual layers, and  
the interlayer having a surface comprising a matrix of islands of remaining material of substantially uniform height with voids extending between these islands.

30. (New) The leadframe as claimed in claim 29, wherein in that the interlayer comprises silver, a silver alloy and/or a silver compound and/or nickel.

31. (New) The leadframe as claimed in claim 29, comprising wherein the surface of the interlayer typically has a roughness average Ra of between approx. 0.1  $\mu\text{m}$  and approx. 0.9  $\mu\text{m}$ , preferably between approx. 0.1  $\mu\text{m}$  and approx. 0.5  $\mu\text{m}$ .

32. (New) The leadframe as claimed in one of claim 29, comprising wherein the remaining islands at the surface of the interlayer typically have a mean diameter of approx. 0.5  $\mu\text{m}$ .

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33. (New) The leadframe as claimed in one of claim 29, comprising wherein the voids at the surface of the interlayer typically have a mean width of approx. 2  $\mu\text{m}$ .

34. (New) The leadframe as claimed in one of claim 29, comprising wherein the surface of the interlayer typically has a ratio of the surface areas of islands to voids in the range from approx. 2:1 to approx. 1:2.

35. (New) A semiconductor device comprising:  
a semiconductor chip and having an encapsulation of plastic compound;  
a leadframe which is configured to be fitted with the semiconductor chip and to be encapsulated with the plastic compound, the leadframe comprising a metallic single-piece base body of a leadframe, at least one interlayer which has been applied to the base body and may comprise one or more individual layers, and  
the interlayer having a surface comprising a matrix of islands of remaining material of substantially uniform height with voids extending between these islands.

36. (New) The semiconductor device as claimed in claim 35, comprising wherein the interlayer comprises silver, a silver alloy and/or a silver compound and/or nickel.

37. (New) The semiconductor device as claimed in claim 35, comprising wherein the surface of the interlayer typically has a roughness average Ra of between approx. 0.1  $\mu\text{m}$  and approx. 0.9  $\mu\text{m}$ , preferably between approx. 0.1  $\mu\text{m}$  and approx. 0.5  $\mu\text{m}$ .

38. (New) The semiconductor device as claimed in one of claim 37, comprising wherein the remaining islands at the surface of the interlayer typically have a mean diameter of approx. 0.5  $\mu\text{m}$ .

39. (New) The semiconductor device as claimed in one of claim 38, comprising wherein the voids at the surface of the interlayer typically have a mean width of approx. 2  $\mu\text{m}$ .

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40. (New) The semiconductor device as claimed in claim 39, comprising wherein the surface of the interlayer typically has a ratio of the surface areas of islands to voids in the range from approx. 2:1 to approx. 1:2.

41. (New) A leadframe which is intended to be fitted with a semiconductor chip and to be encapsulated with a plastic compound, the leadframe having the following features:

a metallic single-piece base body of a leadframe,

means for providing at least one interlayer which has been applied to the base body and may comprise one or more individual layers, and

the interlayer means having a surface comprising a matrix of islands of remaining material of substantially uniform height with voids extending between these islands.